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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,627	05/24/2001	Nobuaki Hashimoto	109609	3172

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EXAMINER

SOWARD, IDA M

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 05/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/856,627

Applicant(s)

HASHIMOTO

Examiner

Ida M Soward

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 24 May 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 and 6.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## DETAILED ACTION

This office action is in response to the preliminary amendment filed on May 24, 2001.

### ***Specification***

The disclosure is objected to because of the following informalities: "This application is a 371 of PCT/JP00/06624 09/29/2000" should appear on the first page of line one of the specification.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The wording of the claim makes the meaning of the claim unclear.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salatino (5,117,282).

As best understood, Salatino teaches an interconnect substrate **61** over which an interconnect pattern is formed, comprising: a first portion **21**-; and a second portion **22**- to be superposed on the first portion, wherein the first portion has an end part as a positioning reference; wherein the second portion has a shape so as to be superposed on the first portion except the end part **25**; the end part as the positioning reference includes two edges that are perpendicular to each other; the first portion comprises a rectangular body section and a projected section **111** which extends from at least one edge of the body section and includes the end part (Figures 1-5); the projected section is a region determined by: an edge which is a boundary between the projected section and the body section; a first edge which is perpendicular to the edge as a boundary; and a second top edge which is parallel to the edge as a boundary, wherein the end part as a positioning reference includes the first and second edges; the body section **27** of the first portion includes an edge having no projected section; and wherein the second portion is disposed adjacent to the edge having no projected section; the second portion has a depressed section **24** facing the projected section of the first

Art Unit: 2822

portion; the first portion has a plurality of the end parts **23** & **25** as positioning references; and wherein at least one of the end parts is formed from an area in the body section other than an area from which the projected section extends; the first portion (which includes the middle section of Figure 1) is larger than the second portion, and the two edges which are perpendicular to each other form a corner section of the first portion; the first portion has a depressed end part (area **23**) including the two edges which are perpendicular to each other and have a right angle; a plurality of holes **18** & **19** formed in end parts; the second portion continuously extends from the first portion; the second portion is separated from the first portion (Figure 1); and wherein the first and second portions are connected by the interconnect pattern (Figure 4); a semiconductor device comprising: at least one semiconductor chip **69**; and a substrate **61** which has a first portion and a second portion to be superposed on the first portion, and on which the semiconductor chip is mounted, wherein the first portion includes an end part as a positioning reference; and wherein the second portion has a shape which avoids being superposed over the end part of the first portion; and a plurality of external terminals **83** are provided in the first portion. In regard to the functional language "as a position reference", claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, *In re Danly*, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). In regard to claims 18-20, note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190

Art Unit: 2822

USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 96 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or no. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP 2113. However, Salatino fails to teach an electronic instrument provided with the semiconductor device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide an electronic instrument with the semiconductor structure of Salatino in order to utilize the integrated circuit devices.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to interconnect substrates:

Arnold et al. (US 6,376,352 B1)

Chia et al. (6,057,594)

Terrill et al. (6,069,026)

Wilson et al. (5,646,068).


Art Unit: 2822

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-3308. The examiner can normally be reached on Monday - Friday, 7:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ims  
May 6, 2002

  
CARL WHITEHEAD, JR.  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800